

DSTATCOM Based Novel Multilevel Inverter Employing Additive and Subtractive Topology for Improving Power Quality

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Abstract

In this paper, a DSTATCOM based novel multilevel inverter is proposed in which it employs additive and subtractive topology to get higher output levels. This approach significantly reduces the number of power switches needed as compared to existing topology. The present developed multilevel inverter can generate only five voltage levels. With this proposed topology the multilevel inverter can be modified to nine level inverter. Moreover modified hybrid multicarrier Pulse Width Modulation (PWM) technique can be implemented in the proposed multilevel inverter in order to obtain uniform switch utilization and lower THD. An appropriate modulation scheme is presented and also the proposed concept is analyzed through simulation studies and the hardware model also tested. The results show that the proposed DSTATCOM based multilevel inverter has successfully improved the power quality.

Key words: DSTATCOM, *Multilevel Inverter (MLI)*; *Pulse Width Modulation (PWM)*; *Multicarrier PWM scheme*; *Additive and Subtractive topology*; *Total Harmonic Distortion (THD)*.

INTRODUCTION

Over the past few decades, multi-stage voltage source inverters have emerged as viable solutions for high-power direct current (DC) to alternating current (AC) conversion applications. A multi-level inverter (MLI) is a multi-input DC level (obtained from a DC source or capacitor) and interlocking structure of a power semiconductor device, and synthesizes a step waveform. In MLIs voltage stresses experienced by the power switches are lower as compared to the conventional inverters. In addition, the multilevel waveform has a better harmonic profile as compared to a two-level waveform obtained from conventional inverters. Other advantages of MLIs are reduced dv/dt stress on the load and possibility of fault-tolerant operation. Researchers are also exploring avenues to employ MLIs for low- Power application. Increasing the number of levels improves the quality of the multi-step waveform. However, it is conversely connected to the gate driver circuit associated with a number of power semiconductor devices. This tends to increase the complexity and cost of the system and reduce the reliability and efficiency of the system. So, for high resolution waveforms, a practical consideration is the need to reduce the number of switch and gate driver circuits

The topologies which have been extensively studied and are commercially available for multilevel voltage output are Neutral Point Clamped (NPC), Cascaded H-Bridge (CHB) and Flying Capacitor (FC) converters. However, there is a significant increase in the number of power switches, the number of switches conducting simultaneously and the overall cost of the system with the increase in the number of output levels. Researchers therefore continue to focus on reducing the component count in multilevel topologies through various approaches. These approaches can be classified into three categories such as topological changes use of asymmetric sources, combination of topological changes and asymmetric source configurations. Here a topology is developed in which alternate DC

sources are linked in opposite polarities via power switches. This approach significantly reduce the number of power switches needed as compared to the classical topologies. Moreover for symmetric input DC sources. The proposed topology shows similarities with the CHB topology in two respects, including the need for multiple isolated input DCs. voltages and input DC voltage levels can be combined into all additive values. Thus the topology can be used as a utility interface for renewable energy systems where a large number of isolated DC sources are available. It can also be used in high voltage drive applications where there are multiple secondary side phase change transformers. windings is generally employed (mainly for the reduction of line current distortion), thus providing isolated DC sources. The switched DC source topology may also be appropriate for battery-powered applications (such as electric vehicles and submarine propulsion). However the switched DC source topology have several drawbacks. So to nullify these drawbacks here proposing a new topology known as "Additive and Subtractive" topology. The working principle of Additive and Subtractive The topology is built using single-phase inverters of 9 levels. Control scheme based on multi-carrier pulse width modulation (PWM) is described for the inverter and simulation results are presented. In addition to this comparison of the proposed topology with the existing topology is also presented. Lastly the possible modifications that can be implemented to this newly developed MLI is addressed.

Recently multilevel inverters are gaining popularity due to reduced voltage stress across power switches and low Total Harmonic Distortion (THD) output voltage waveform. Multilevel converters offer high power capability, associated with lower output harmonics and lower commutation losses Their main disadvantage is their complexity, requiring a great number of power devices and passive components and a rather complex control circuitry. This work reports a new MLI

with additive and subtractive topology to reduce the number of switching devices. This also helps in reduction of the manufacturing cost. The main objective of this project is to design a single-phase nine-level MLI with reduced number of components. This topology reduces the harmonic components of the output voltage and the load current. It requires fewer switch compared to existing inverters and requires fewer gate drivers and carrier signals. This topology and modulation techniques used will minimize the THD and switching stresses. Standard cascaded MLI requires “n” number of DC sources for “2n+1” levels. In actual practice four H-bridges to be cascaded to obtain nine levels. This project proposes a novel multilevel inverter with additive and subtractive topology which generates nine level output and also a comparison is made between the proposed and existing MLI.

REVIEW ON MULTI LEVEL INVERTERS

Nowadays, uses of inverters are widely increasing. There are applications varying from medium voltage to high voltage high power applications which require DC to AC conversion. The following papers are referred which were published in various journals and conference proceedings to have the idea about MLIs. **M. Manjrekar and G. Venkataramanan**[1] Introduced and studied about various topologies to realize the multilevel inverters. Here presents the development of real-time voltage control techniques for multilevel inverters based on multilevel sigma delta modulators. The spectral performance of the output waveforms is investigated. Various design criteria, performance characteristics, comparison with existing modulation methods and other practical issues are discussed. **B. P. McGrath and D. G. Holmes**[2] Evaluated the PWM strategy analysis solution of multi-stage NPC and cascade inverter. These solutions show that the Alternative Phase Opposition Disposition (APOD) PWM strategy of NPC inverters produces the same spectral components as the

phase shift carrier PWM strategy of cascade inverters. Adjust the carrier frequency so that each switch has the same number of transitions. Inverter spanning one fundamental cycle. Thus a new method is proposed to apply the harmonically superior Phase Disposition (PD) PWM strategy for NPC inverters to cascaded inverters, to achieve improved harmonic performance for the modulation of cascaded inverters. **Jose Rodriguez et al**[3] Presented a brief summary of multilevel inverter topologies and their control strategies. Here the most important topologies like diode-clamped inverter (neutral-point clamped), capacitor-clamped (flying capacitor), and cascaded multilevel with separate dc sources are discussed. New topologies such as asymmetric hybrid cells and soft-switch multi-level inverters are discussed. This white paper also describes the most relevant control and modulation schemes: multi-level sinusoidal pulse width modulation, multi-step selective harmonic rejection, and space vector modulation. Particular attention is paid to applications where laminators, conveyor belts, integrated power flow controllers, etc. are more relevant than the latest triumph of converters. **Steffen Bernet et al**[4] Studied the Neutral Point Clamped MLI topology for high power applications (several megawatts). Here the basic operation of multilevel inverter and the most used modulation and control techniques are presented. An active NPC inverter is presented to overcome the loss distribution in semiconductors. Classical pulse width modulation and Space Vector Modulation (SVM) have been the preferred modulation techniques for operation with low switching frequency. The field of application of NPC inverters is permanently growing due to their compactness, efficiency, and good performance. Here it also provide the main fields of application and presents some technological problems such as capacitor balance and losses. **Pablo Lezana et al**[5] Illustrated the faults that can appear in multilevel inverters, which have a high number of components. Methods for identifying failures are categorized by topology and are easily described. Also, some strategies and hardware modifications that allow for operation

in faulty conditions are also presented. The availability of powerful microprocessors permitted the development of very intelligent strategies to identify faults quickly, using a reduced number of sensors, by measuring the converter output signals (voltage or current in the load). **Samir Kouro *et al.*** [6] In their articles it deals with the new converters for industrial applications. The purpose of this white paper is to group and review these recent contributions of multi-level inverters in industrial applications. Introducing an overview of proven multi-level converters that are strongly oriented towards the current state of industrial applications. In addition to these new promising topologies are discussed. Most of this research article is focused on non-traditional applications with multi-level converters and showing how multi-level converters are becoming a realization technology in many industries. Recent advances opened in modulation and control of multi-level converters are also discussed. **Sara Laali *et al.*** [7] Illustrated multi-carrier PWM techniques for multilevel inverters and several interesting characteristics of them are revealed. A new method of multi-carrier PWM strategies is also developed and compared with different conventional multi-carrier PWM techniques. Reduction of THD and improvement of the harmonic spectrum of inverter output voltage are some advantages of the developed control method. The simulations are carried out to validate the capabilities of the developed modulation method. **K.K. Gupta and S. Jain** [8] Described about a novel multilevel topology, where This topology allows you to get all the addition and subtraction combinations of the input DC level of the output waveform. The number of levels depends on the DC source array. Appropriate modulation schemes were also used for low switching frequency operation in multi-level topologies. Compared to existing multi-level topologies, the developed topology reduces the number of switches and conduction loss. The operation and performance of this multi-level converter was confirmed by simulation and experimentally verified with a single-phase 9-level multi-level inverter. When compared to the classic topologies, the device count is significantly reduced for a given

number of levels in the output. A charge balance control scheme has also been investigated with a 15-level inverter based on the proposed structure with asymmetric source configuration. **Adithya S N and Raghu Raman S** [9] Evaluated the most commonly used multilevel sinusoidal pulse width modulation techniques are evaluated. It comprises of Phase Disposition (PD), Alternative Phase Opposition Disposition (APOD) & Phase Opposition Disposition (POD) methods. Various factors such as amplitude modulation index, frequency modulation index, phase angle between carrier and reference modulating wave have been considered for simulation purposes. Variation in these factors and their effect on inverter performance is evaluated. Factors such as DC bus utilization, output r.m.s voltage, Total Harmonic Distortion (THD), dominant harmonic order and switching losses are evaluated based on simulation results. Comparison of each techniques have been carried out. **Sruthi C K and Saritha P** [10] In their This article focused on a multi-level inverter with 9 levels of DC link capacitors on the input side. The main drawback of cascading multi-level inverters is the number of DC sources. Therefore, a 9-level multi-level inverter with a DC link switch requires a smaller number of DC sources than a traditional multi-level inverter. Here a modulation technique single carrier method is employed and the feasibility of the proposed nine level inverter is verified through certain methods. **Zahra Malekjamshidi *et al.*** [11] Studied and discussed about the characteristics of main topologies of voltage source multilevel inverters. The selected topologies included conventional two levels, flying capacitor, neutral point clamped and three level cascaded H-bridge inverters. Several performances of topologies including quality of waveforms of output voltage, cost, complexity and reliability are selected as indicators for comparative study. Based on the study it can analyse that CHB topology showed the highest cost and complexity and the lowest THD and reliability compared with others. On the other hand 2-level topology presents the highest THD of output voltage with the least complexity.

Indrajit Sarkar and B.G. Fernandes[12] Demonstrated a new modified hybrid pulse width modulation technique. Performance of Phase Shift PWM (PS-PWM), Carrier Disposition PWM (CD-PWM) and Hybrid PWM techniques was evaluated. Hybrid PWM technique is the superior technique over all other techniques. Fixed CD PWM and Hybrid PWM technology can be used to mitigate problems associated with non-uniform power distribution. Low modulation index, line voltage and line current THD are less hybrid PWM technology compared to PS PWM and modified CD PWM technology. A 7-level CHB multilevel inverter is simulated in MATLAB/Simulink and the line voltage and current waveforms at different modulation indices are presented. It is found that for equal device switching frequency, the overall performance of Hybrid-PWM technique is superior to that with PS-PWM and Modified CD-PWM techniques. **Olive Ray et al.**[13] Discussed about a family of Single Input Multiple Output (SIMO) DC-DC converter topologies, with this topology it can provide one step up and multiple step down outputs. These topologies are synthesized by replacing the control switch of a boost converter topology with series-connected switches and using the additional switch nodes to generate step-down dc outputs. Compared with separate converters, these topologies utilize a lower number of switches and are more reliable due to their inherent shoot through protection. The steady-state characteristics and dynamic behaviour of the converter have been studied. **Alex Ruderman**[14] Studied about the voltage total harmonic distortion in multilevel inverters. Studies shows that Given a numerically calculated (measured) voltage THD value that can cause calculation errors, it can be difficult to judge for multiple levels of voltage quality. Here are some simple smoothed hyperbolic voltage THD upper and lower bound approximations for single-phase and three-phase inverters that use the closest synchronous switching. This is useful for counting any modulation index and evenly distributed levels and can actually be used as a good reference value. Line and Phase Voltage THD for Balanced Loads with Insulated Neutral and

Phase Symmetric Modulation in Three-Phase Star Connection are basically the same independent on a multilevel inverter type employed. As the major multilevel voltage quality improvement comes from increased levels count, Selected Harmonics Elimination and similar techniques. **Tila Muhammad et al.**[15] Studied and discussed about the isolated DC voltage sources for multilevel inverters. Here the isolated DC supplies have been generated from a single voltage source. The conversion has been done using ferrite core high frequency transformer. It is found that the DC source can easily be split into a number of isolated DC Sources as per desire by using less in system losses, small size and weight of the converter. This became in benefit of small size and cost effectiveness. The in-system losses have decreased which results in increase of efficiency.

DESIGN OF DSTATCOM BASED MULTILEVEL

A D-STATCOM is a distributed static compensation device that uses a two-level voltage source converter (VSC) to convert a single DC voltage to three-phase ac outputs. The VSC is commonly used for controlling the flow of active and reactive power in a network. It consists of a storage device and a coupling transformer.

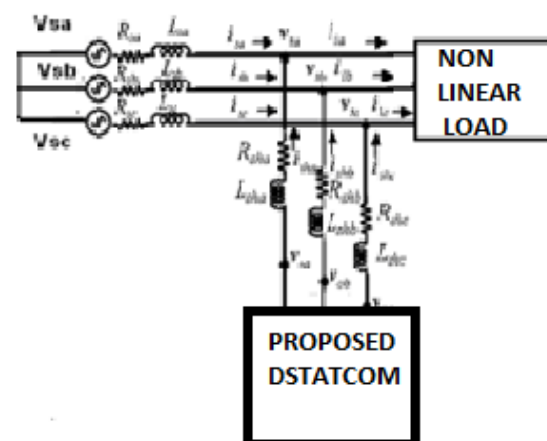


Fig. 1 Schematic Diagram of a DSTATCOM

The VSC is connected in parallel with ac system as shown in fig.1. Its provide three main function: 1. Reactive power compensation and regulation of voltage; 2. Power factor correction 3. Current harmonics elimination

MULTILEVEL INVERTER USING ADDITIVE AND SUBTRACTIVE TOPOLOGY

Today, MLI is becoming more popular with reduced voltage stress across power switches and low THD output voltage waveforms. But as the level increases, so does the equipment. Therefore, we now propose a new topology known as the subtraction topology, which we add to get the maximum level number of output voltage waveforms as a limited number of components. With this topology it is capable of obtaining all additive and subtractive combinations of input DC levels in the output voltage waveform. The DC sources and switches are arranged so that you can get all possible combinations of outputs. i.e., if 'n' number of DC sources are present, then '4n' power switches are required to obtain all possible combinations. From this concept for the proposed topology total number of power switches required is '4n'. Some examples of possible additive and subtractive combinations of the DC levels combinations are as follows:

(a) With Single DC Source:

If a single DC source of voltage E_1 is present, the possible combinations are: $+E_1$, 0 and $-E_1$. The resultant inverter can be a three level or two-level (when zero level is excluded) inverter.

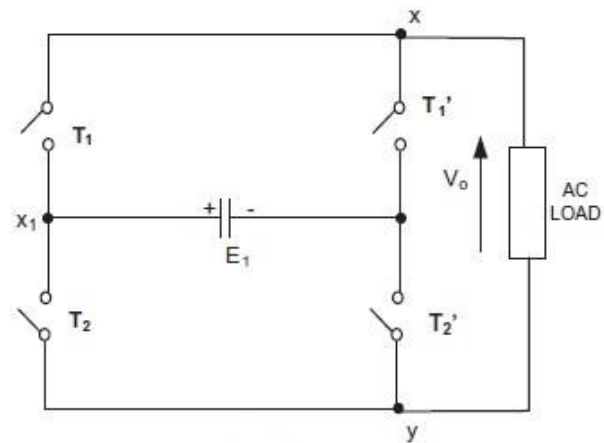


Fig.2 Inverter Structure with Single DC Source

Such a structure is shown in fig.2. It is a standard single-phase full bridge inverter.

(b) With two DC sources:

If two DC sources with voltages E_1 and E_2 are present, the possible combinations are:

(i) Taking one level at a time: E_1 , E_2 , $-E_1$ and $-E_2$

(ii) Taking two levels at a time: $(E_1 + E_2)$, $(E_1 - E_2)$, $(E_2 - E_1)$ and $(-E_1 - E_2)$

(iii) Zero level: one

Thus with two DC sources, there are nine possible combinations that can be obtained in the output waveform, resulting in a nine level inverter. Such a structure is shown in fig.3.

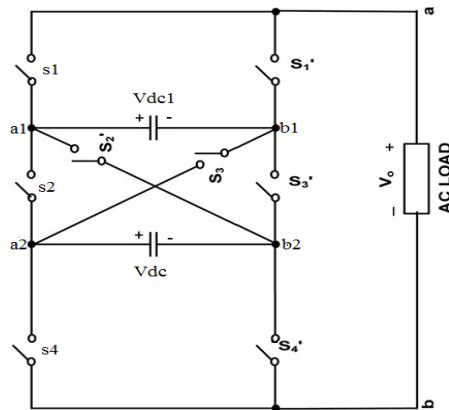


Fig.3. Inverter Structure with Two Input DC Sources

(c) With Three DC Sources:

Given the presence of three DC supplies of voltages E_1 , E_2 and E_3 , the possible combinations are:

(i) Have one level at a time: E_1 , E_2 , E_3 , E_1 , E_2 , E_3 .

(ii) has two levels at once: $(E_1 + E_2)$, $(E_1 E_2)$, $(E_2 E_1)$, $(E_1 E_2)$, $(E_2 + E_3)$, $(E_2 E_3)$ $(E_3 E_2)$, $(E_2 + E_3)$, $(E_1 + E_3)$, $(E_1 E_3)$ $(E_3 E_1)$ and $(E_1 + E_3)$.

(iii) has three levels at once: $(E_1 + E_2 + E_3)$, $(E_1 + E_2E_3)$, $(E_1 E_2 + E_3)$, $(E_1 E_2E_3)$, $(E_1 + E_2 + E_3)$, $(E_1 + E_2 E_3)$, $(E_1 E_2 + E_3)$ and $(E_1 + E_2 + E_3)$.

(iv) Zero Level: One

Therefore, with three DC sources, there are 27 additive and subtractive combinations possible which result in a 27 level inverter.

(d) With 'n' number of DC sources:

A generalized structure can be obtained for 'n' number of DC sources. If 'n' number of DC sources with voltages E_1 , E_2 , E_3 , ..., E_n are present then the number of possible combinations can be obtained by proceeding in the same manner as done for one, two and three and taking 'm' number of sources at a time, where 'm' varies from 1 to 'n'. The generalized structure for the proposed single phase inverter is shown in fig.4.

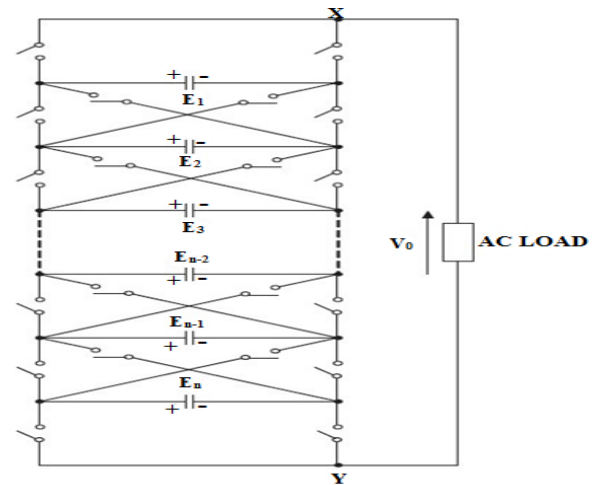


Fig.4. Proposed Single Phase Structure with 'n' DC Sources

Principle

The working principle of the proposed topology is explained with the help of a single-phase 9-level inverter. It consists of two input asymmetric DC sources E_1 and E_2 so that $E_2 < E_1$ as shown in Figure 4. The DC source array is chosen so that $E_1 / E_2 = 3$. Therefore, this configuration can generate nine output voltage levels. DC sources can be organized in several ways:

(i) If all DC sources are the same, a "unary" array is created. That is,

$$E_1 = E_2 = E_3 = \dots = E_n$$

(1)

(ii) The "binary" array has a geometric progression with the DC source as an argument of "1/2". Occurs when. That is,

$$E_1 / E_2 = E_2 / E_3 = \dots = E_{n-1} / E_n = 2$$

(2)

(iii) If the DC source geometrically advances to a coefficient of "1/3", then "A triple" array is created. That is,

$$E1 / E2 = E2 / E3 = \dots = 3$$

(3)

In this topology the two sources are $E2$ & It ; $E1$ and its sequence (unary, binary or ternary) the actual output. Determine the number of levels of. For example, by using two sources $E1$ and $E2$ with the same value ($E1 = E2 = E0$), there are five output levels (ie, that is). You can get $\pm E0, \pm 2E0$ and 0 (that is, a 5-level waveform in the EO stage). Seven output levels (ie $\pm E0, \pm 2E0, \pm 3E0$ and 0) can be combined using the binary source settings ($E1 = 2E0$ and $E2 = E0$) (that is, 7 levels in the EO stage). Waveform). Similarly, a ternary source configuration ($E1 = 3E0$ and $E2 = E0$) synthesizes voltage levels ($\pm E0, \pm 2E0, \pm 3E0, \pm 4E0$ and 0), a 9-level waveform with $E0$ steps.

Operation

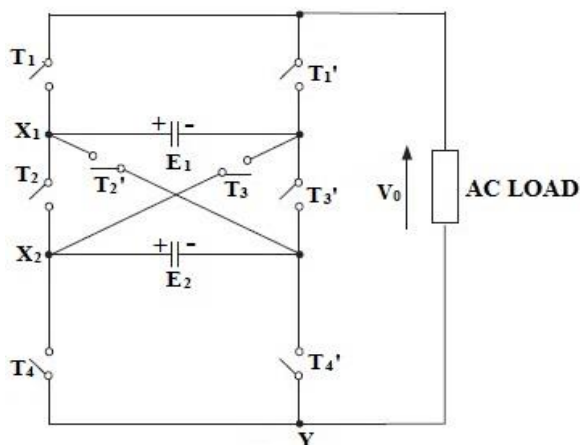


Fig.5. Proposed Single Phase Nine Level Inverter

In practice, a desired source configuration can be easily obtained in applications like renewable energy based power generation (where separate DC sources are available in the form of photovoltaic arrays/modules and/or fuel cells) and AC drives (where multi-winding transformers are often employed and thus isolated DC sources are obtained by

rectification and filtration of secondary voltages).

Power Switch Configuration

The proposed inverter can be realized with self-commutating power switches like MOSFET's and IGBT's. The topology has eight switches and to obtain any desired voltage level, three switches need to be ON simultaneously as observed from fig.6. There are four pairs of complimentary switches. It is also important to note that the switches at positions $T2$ and $T3'$ are necessarily required to be 'fully directional switches' otherwise their undesirable switching will take place. When an output level ($E1 + E2$) is required and switches $T4'$, $T3$ and $T1$ are ON, then the anti-parallel diode of switch $T3'$ gets a forward biasing potential difference of $E2$. Thus it acts as ON switch, thereby short-circuiting the source $E2$. A similar phenomenon happens when switches $T4$, $T2'$, $T1'$ are ON in order to obtain the output level of $-(E1 + E2)$. Under such conditions, the anti-parallel diode of $T2$ gets a forward-biasing potential difference equal to $E2$, thereby short-circuiting the source $E2$. Therefore, at both positions $T2$ and $T3'$, fully directional switches having the capability of blocking voltages in both directions are to be used.

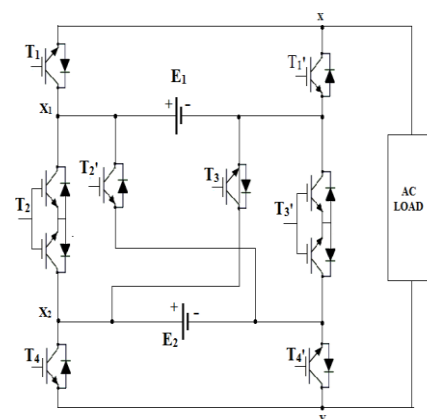


Fig.6. Proposed Configuration for Single Phase Nine Level Inverter

Modes of Operation

Mode 1:

Mode 1 operation is used to obtain output voltage $V_0 = E_1$, where E_1 is the 2nd voltage level of the nine level inverter. In order to obtain this output voltage the switches T_1 , T_3' , and T_4' conducts. Fig.7. depicts the current flow in mode-1 operation. The path of the current flow is such that

$E_1 \rightarrow T_1 \rightarrow \text{LOAD} \rightarrow T_4' \rightarrow T_3' \rightarrow -E_1$.

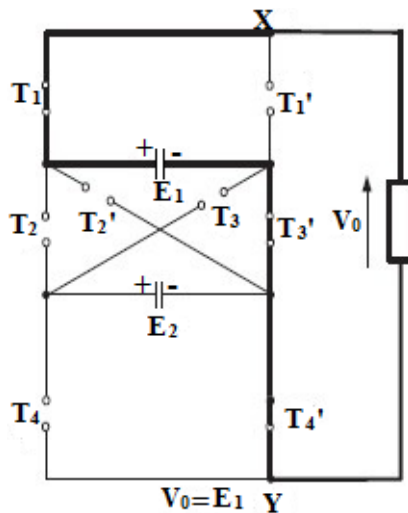


Fig.7. Current Path in Mode 1 Operation

Mode 2:

Mode 2 operation is used to obtain output voltage $V_0 = E_2$, where E_2 is the 4th voltage level of the nine level inverter. In order to obtain this output voltage the switches T_1' , T_3 , and T_4' conducts. Fig.8. depicts the current flow in mode-2 operation. The path of the current flow is such that

$E_2 \rightarrow T_3 \rightarrow \text{LOAD} \rightarrow T_4' \rightarrow T_1' \rightarrow -E_2$.

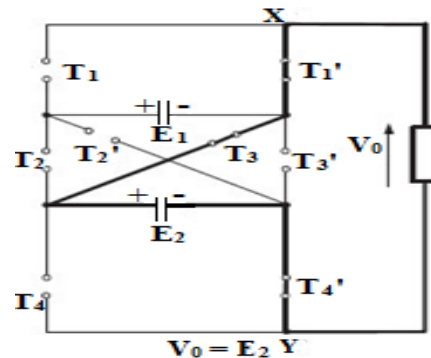


Fig.8. Current Path in Mode 2 Operation

Mode 3:

Mode 3 operation is used to obtain output voltage $V_0 = E_1 - E_2$, where $E_1 - E_2$ is the 3rd voltage level of the nine level inverter. In order to obtain this output voltage the switches T_1 , T_3' , and T_4 conducts. Fig.9. depicts the current flow in mode-3 operation. The path of the current flow is such that

$E_1 \rightarrow T_1 \rightarrow \text{LOAD} \rightarrow T_4 \rightarrow E_2 \rightarrow T_3' \rightarrow -E_1$.

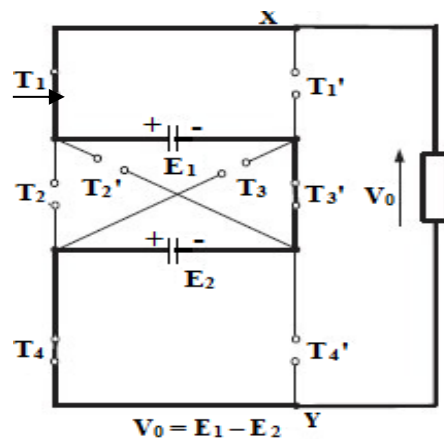


Fig.9. Current Path in Mode 3 Operation

Mode 4:

Mode 4 operation is used to obtain output voltage $V_0 = E_1 + E_2$, where $E_1 + E_2$ is the first voltage level of the nine level inverter. In order to obtain this output voltage the switches T_1 , T_3 ,

and T_4' conducts. Fig.10. depicts the current flow in mode-4 operation. The path of the current flow is such that

T_1 \rightarrow LOAD \rightarrow T_4' \rightarrow $-E_2$ \rightarrow $+E_1$ \rightarrow T_3 \rightarrow $-E_1$.

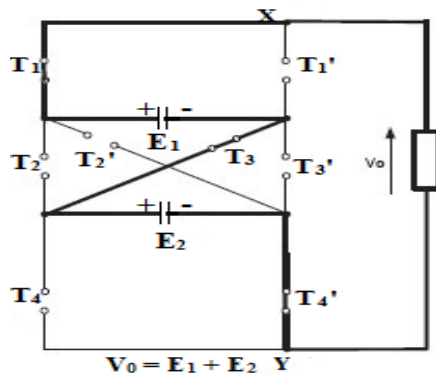


Fig.10. Current Path in Mode 4 Operation

Mode 5:

Mode 5 operation is used to obtain output voltage $V_0 = 0$, where 0 is the 5th voltage level of the nine level inverter. In order to obtain this output voltage the switches T_1' , T_3' , and T_4' conducts. Fig.11. depicts the current flow in mode-5 operation. The path of the current flow is such that

$\text{LOAD} \rightarrow T_4' \rightarrow T_3' \rightarrow T_1'$.

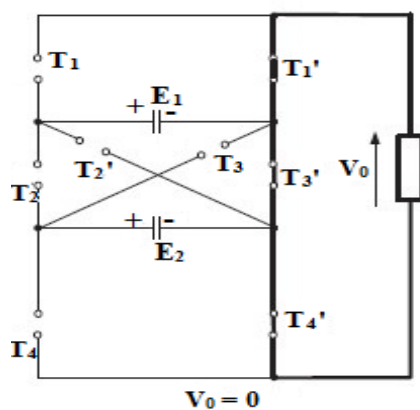


Fig.11. Current Path in Mode 5 Operation

Mode 6:

Mode 6 operation is used to obtain output voltage $V_0 = -E_1$, where $-E_1$ is the 8th voltage level of the nine level inverter. In order to obtain this output voltage the switches T_2 , T_4 , and T_1' conducts. Fig.12 depicts the current flow in mode-6 operation. The path of the current flow is such that

$T_2 \rightarrow T_4 \rightarrow \text{LOAD} \rightarrow T_1' \rightarrow -E_1$.

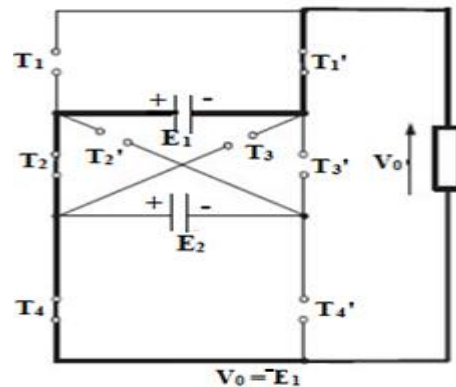


Fig.12 Current Path in Mode 6 Operation

Mode 7:

Mode-7 operation is used to obtain output voltage $V_0 = -E_2$, where $-E_2$ is the sixth voltage level of the nine level inverter. In order to obtain this output voltage the switches T_1' , T_3 , and T_4 conducts. Fig.13. depicts the current flow in mode-7 operation. The path of the current flow is such that

$T_4 \rightarrow \text{LOAD} \rightarrow T_1' \rightarrow T_3 \rightarrow -E_2$.

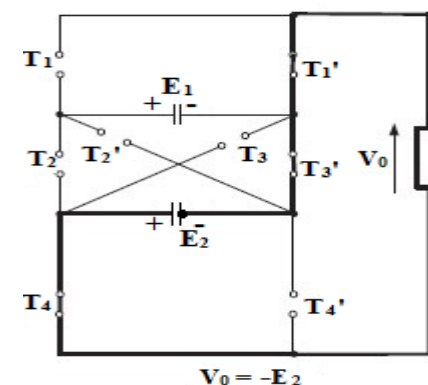


Fig.13. Current Path in Mode 7 Operation

Mode 8:

Mode 8 operation is used to obtain output voltage $V_0 = E_2 - E_1$, where $E_2 - E_1$ is the seventh voltage level of the nine level inverter. In order to obtain this output voltage the switches T_1' , T_2 , and T_4' conducts. Fig.14. depicts the current flow in mode-8 operation. The path of the current flow is such that

$$\begin{array}{l} T_2 \rightarrow E_1 \rightarrow E_1 \rightarrow T_1' \rightarrow \text{LOAD} \rightarrow E_2 \\ -E_2 \rightarrow T_4' \end{array}$$

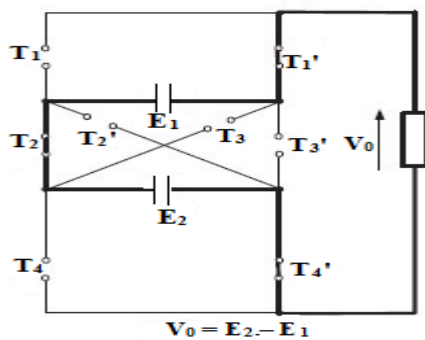


Fig.14. Current Path in Mode 8 Operation

Mode 9:

Mode 9 operation is used to obtain output voltage $V_0 = -E_1 - E_2$, where $-E_1 - E_2$ is the 9th

voltage level of the nine level inverter. In order to obtain this output voltage the switches T_1' , T_2 , and T_4' conducts. Fig.15. depicts the current flow in mode-9 operation. The path of the current flow is such that

$$\begin{array}{l} T_1' \rightarrow \text{LOAD} \rightarrow T_4 \rightarrow E_2 \rightarrow E_2 \rightarrow T_2' \rightarrow \text{LOAD} \rightarrow T_1' \\ +E_1 \end{array}$$

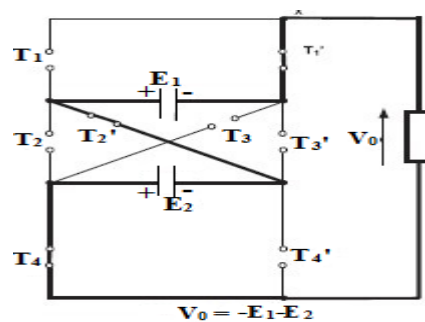


Fig.15. Current Path in Mode 9 Operation

SIMULATION AND EXPERIMENTAL ANALYSIS

The existing multilevel inverter topology can be modulated with multicarrier PWM scheme. The modulation scheme for the five level inverter is shown in fig 16 . The multi-carrier PWM method is used in switching devices where the carrier signal is compared with a reference signal and the pulses obtained correspond to each voltage level. This modulation scheme results in a comparison of the reference sine wave to all carrier waveforms above the time axis, resulting in either a "1" or a "0". Comparison of the reference sine wave to all carriers below the time axis is either '0' or '1'

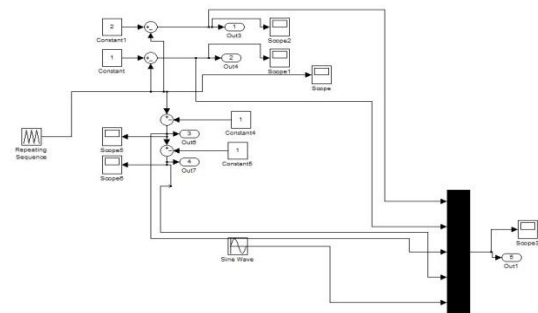


Fig.16. Model of Modulation Control Technique for Five Level Inverter

The switching signals for the switches are obtained from the aggregate signal. The switching signals thus obtained are known as D-states. Thus D-states are generated by combining it with switching pattern and saturation limits. A one-to-one relationship of the levels contained in aggregated signal with corresponding levels in the output waveform is utilized to obtain switching pulses from the aggregate signal. To do so, aggregate signal is compared with constant levels, and the output is fed to switches corresponding to the level needed. The model of aggregate signal is shown in fig.17.

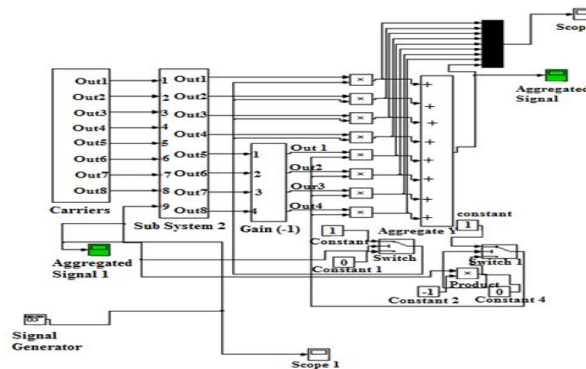


Fig.17. Model of Aggregate Signal Formation for Five Level Inverter

To examine the performance of this existing topology and the control scheme, a simulation model of a single-phase five level inverter is developed with MATLAB/Simulink tool. Two input DC sources such as $E_1 = E_2 = 100$ V are used. Here this simulation model consists of modulation control circuit, pulse generation and power circuit. By simulating the model a voltage of ± 200 V is generated. The overall simulation model for the five level inverter is shown in fig.18.

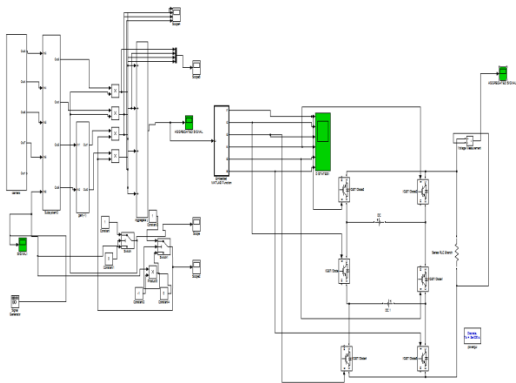


Fig.18. Overall Model of single phase Five Level Inverter

Model of Nine Level Inverter Using Switched DC Source Topology

Develop simulation models of single-phase 9-level inverters using MATLAB/Simulink tools to explore the performance of conventional topologies and control schemes. $E_1 = E_2 = E_3 = E_4 = 50$ V, etc. 4 input DC power is used. By

simulating the model, a voltage of ± 200 V is generated. An overall simulation model of a 9-level inverter is shown in Figure 19.

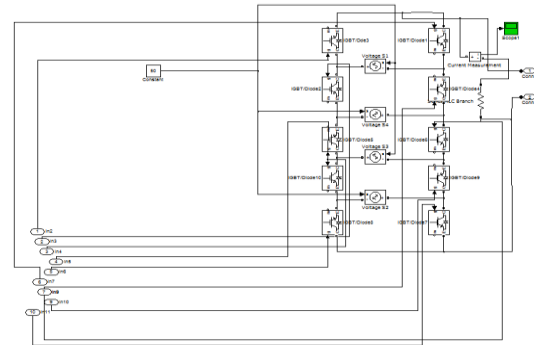


Fig.19. Model of single phase Existing Nine Level Inverter

Model of Nine Level Inverter Using Additive and Subtractive Topology

The control over the control of the proposed structure is represented by a low switching frequency multi-carrier scheme. The multi-carrier PWM method is used in a switching device in which the carrier signal is compared with a reference signal and the pulse thus obtained corresponds to each voltage level. However, in the proposed structure, the various switches do not work independently of each other. Therefore, the signal obtained from the comparison of career and reference cannot be fed directly to the switch as in the case of a two-level inverter. The modulation control scheme is shown in Figure 20.

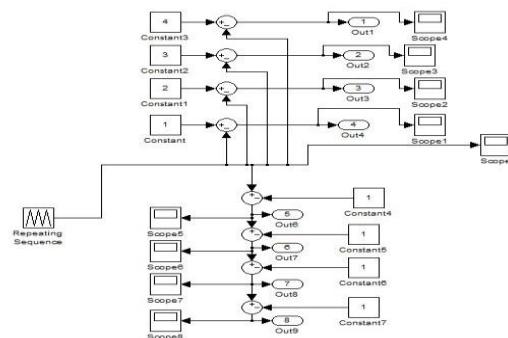


Fig.20. Simulation Model of Pulse Generation for Proposed Nine Level Inverter

The signals obtained from the comparison of carriers and the reference sine wave result in aggregated signal 'As'. The aggregated signal 'As' has same number of levels as desired in the output waveform. The carrier waveforms above the time axis are C_1, C_2, C_3 and C_4 and those below the time axis are C_5, C_6, C_7 and C_8 . The D-State signals are designated $DS_1, DS_2, DS_3, DS_4, DS_5, DS_6, DS_7$ and DS_8 . They are used to obtain output voltage levels 0, E_2 , $(E_1 - E_2)$, E_1 , $(E_1 + E_2)$, $-E_2$, $(E_2 - E_1)$, $-E_1$ and $(E_1 + E_2)$ respectively. The simulation model of D-State generation is shown in fig.21..

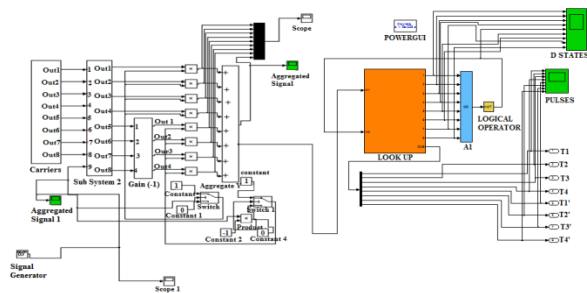


Fig.21. Model of D-State Generation for Proposed Nine Level Inverter

MATLAB Simulink model of the overall simulation model for the modified nine level inverter is shown in fig.22. and it consists of voltage divider, pulse generation and multilevel inverter. The gating signals for all the switches are given by the multicarrier PWM technique.

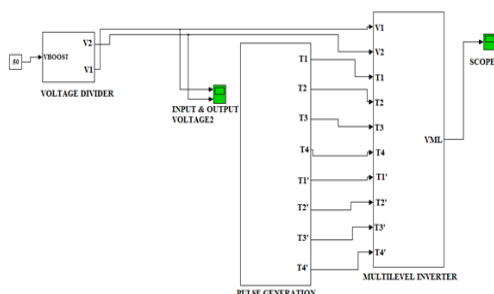


Fig.22. Simulation Model of Modified Nine Level Inverter

Hardware

The control algorithm of nine level inverter is developed using ATMEGA16. The hardware

implementation of the circuit is explained. The switching device used in the circuit is IRFP250N. The circuit parameters were according to the circuit requirement. The AC voltage, typically 230V rms, is connected to a transformer, which steps that AC voltage down to the level of the desired DC output. A diode rectifier then provides a full-wave rectified voltage that is initially filtered by a simple capacitor filter to produce a DC voltage. This resulting DC voltage usually has some ripple or ac voltage variation. A regulator circuit removes the ripples and also remains the same dc value even if the input DC voltage varies, or the load connected to the output DC voltage changes. This voltage regulation is usually obtained using one of the popular voltage regulator IC units. An isolator is provided in between the control unit and the driver circuit for optical isolation and boosting. After regulation 15V AC is given to the power circuit for the switching of MOSFET switches. In the power circuit it consists of eight switches and two DC sources. With the proper switching of these switches nine output voltage levels are developed.

Hardware section of nine level multilevel inverter is shown in fig.23. It has power unit, driver circuit unit and controller unit. The AC input from the main supply is stepped down using a step down transformer. The stepped down AC voltage is converted into DC voltage using a diode bridge rectifier. With a voltage regulator connected to the DC output, the voltage can be maintained. Here L7805 and L7815 voltage regulators are used. L7805 regulator is used in controller unit and L7815 regulator is used in driver circuit. Driver circuit is used to provide sufficient volts to switch the MOSFET switches of the multilevel inverter. Driver amplifies the voltage from microcontroller. Also it has an optocoupler for isolating purpose so damage to MOSFET is prevented.

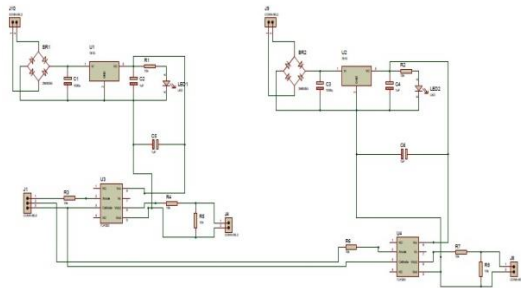


Fig.23. Circuit Diagram of Driver Board

The circuit inside the driver board is shown in fig.24. It consists of full bridge rectifier, optocoupler TLP250 and voltage regulator L7815.



Fig.24. Hardware Section

Hardware section of nine level multilevel inverter consists of supply section, driver circuit, control unit with microcontroller ATMEGA16 and power circuit which is the proposed nine level multilevel inverter, to produce a higher voltage level with reduced component count and lower THDs.

RESULT AND DISCUSSIONS

Five Level Inverter Based on Switched DC Source Topology

The output waveforms for the existing five level inverter obtained is shown in fig. 25. This figure shows the output voltage level

obtained from the multilevel inverter and it also indicate the output voltage obtained from it.

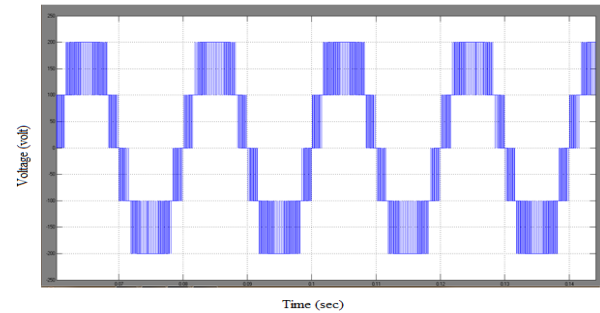


Fig.25. Five Level Output

The fig.26. shows the THD for the output voltage and it is about 27.16% and fig.27. shows the THD for the output current and it is also 27.16%. To get five level at the output the input voltage is given as $E_1 = 100V$ and $E_2 = 100V$ and output voltage is $\pm 200V$. Fig.28. represents the aggregate signals obtained from the modulation scheme.

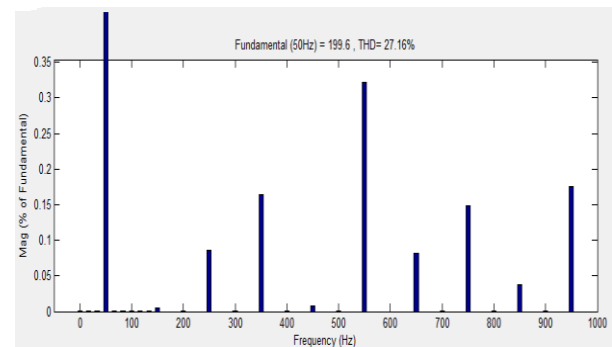


Fig.26. Output Voltage THD for Five Level

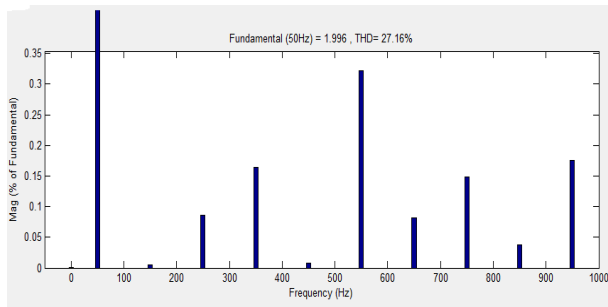


Fig.27. Output Current THD for Five Level

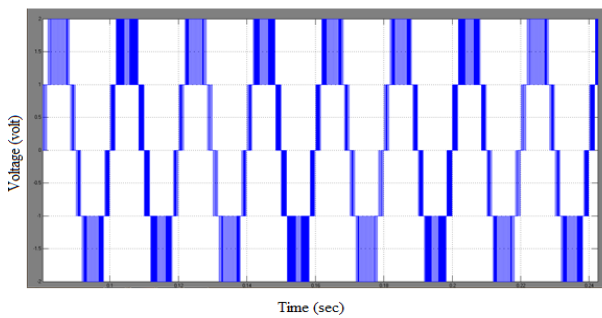


Fig.28. Aggregate Signal for Five Level

Nine Level Inverter Based on Switched DC Source Topology

The output waveforms for the existing nine level inverter employing switched DC source topology is shown in fig.29. This figure shows the output voltage level obtained from the multilevel inverter and it also indicate the output voltage obtained from it.

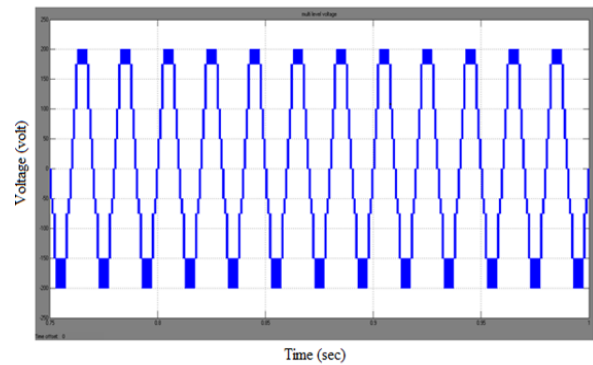


Fig.29. Existing Nine Level Output

To get nine level at the output the input voltage is given as $E_1 = E_2 = E_3 = E_4 = 50V$ and output voltage is $\pm 200V$. The output voltage and current THDs are simulated and it is obtained as 23.89%. The simulated waveforms for THDs are shown in fig.30. and fig 31.

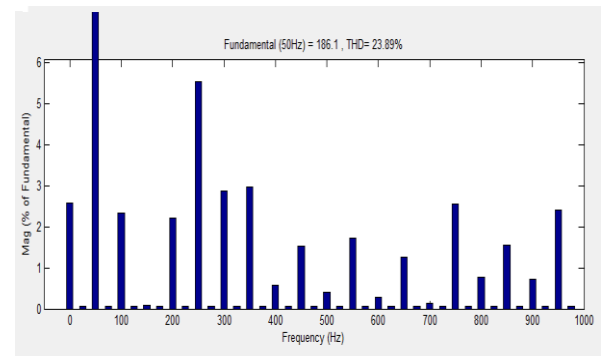


Fig.30. Output Voltage THD for Existing Nine Level

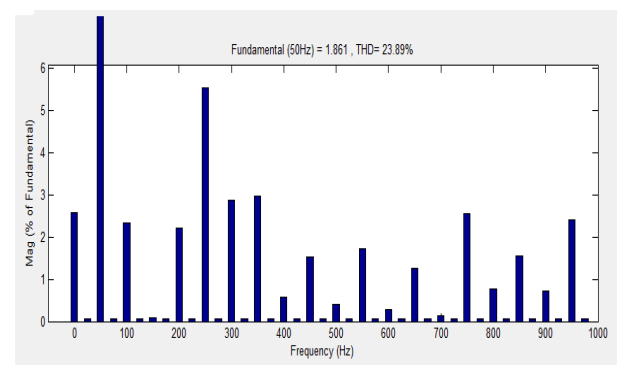


Fig.31. Output Current THD for Existing Nine Level

Nine Level Inverter Based on Additive and Subtractive Topology

The following waveform shows the output of modified nine level inverter and it is shown in fig.32. This figure shows the output voltage level obtained from the multilevel inverter and it also indicate the output voltage obtained from it.

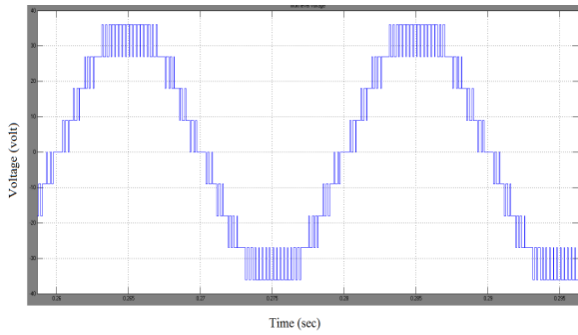


Fig.32. Proposed Nine Level Output

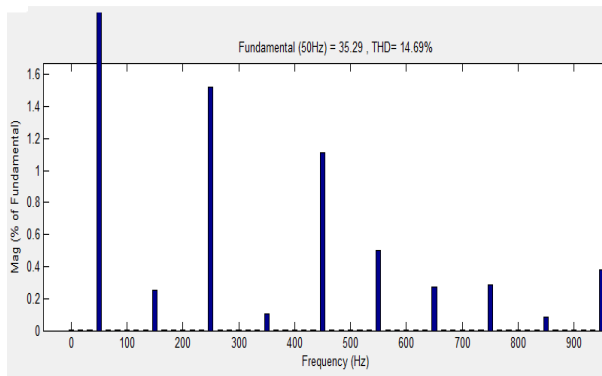


Fig.33. Output Voltage THD for Proposed Nine Level

The fig.33. shows the THD for the output voltage and it is about 14.69% and fig.34. shows the THD for the output current and it is also 14.69%. To get nine level at output the input voltage is given as $E_1 = 9V$ and $E_2 = 27V$ and output voltage is $\pm 36V$. Fig.35. represents the D-States signals obtained from the modulation scheme.

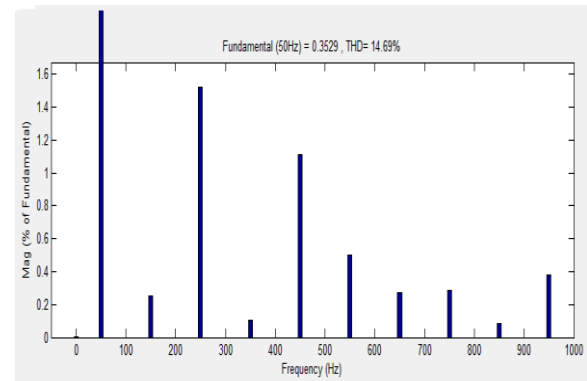


Fig.34. Output Current THD for Proposed Nine Level

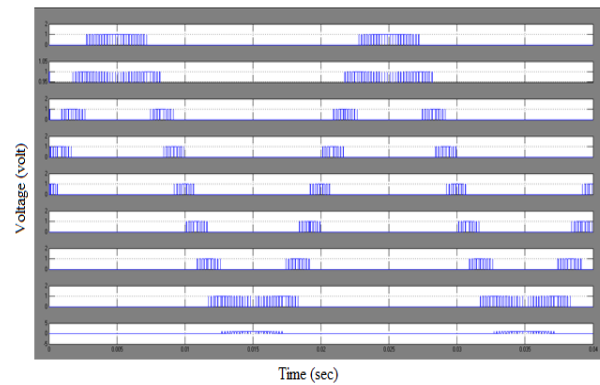


Fig.35. D-States

Comparison of Existing and Modified MLI

By comparing the output waveforms obtained by the modelled systems we can observe that the proposed system gives a higher output voltage levels of nine and lower THDs of 14.69% with lower components count as compared to the existing systems. The comparison of Existing and Modified MLI is shown in table.1.

Table 1 Comparison of Existing and Modified MLI

	Existing MLI	Modified MLI

Parameters for Comparison	Five Level MLI	Nine Level MLI	Nine Level MLI
Input Voltage	$E_1 = E_2 = 100V$	$E_1 = E_2 = E_3 = E_4 = 50V$	$E_1 = 9V,$ $E_2 = 27V$
Output Voltage	$\pm 200V$	$\pm 200V$	$\pm 36V$
Number of Output Voltage Levels	5	9	9
THD for Output Voltage	27.16%	23.89%	14.69%
THD for Output Current	27.16%	23.89%	14.69%
Component Count	2 DC Sources and 6 Switches	4 DC Sources and 10 Switches	2 DC Sources and 8 Switches

Experimental Results

A 9V and 27V battery source is used as the input to the multilevel inverter circuit. A digital storage oscilloscope is used to obtain the signals from each terminal and the obtained waveforms are shown below. The fig.36 shows the output waveform of generated pulse for the switches and fig.37 shows the nine level output of the multilevel inverter prototype.

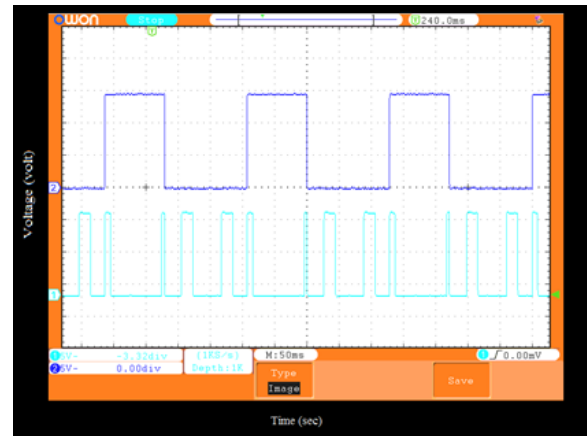


Fig.36. Generated Pulses

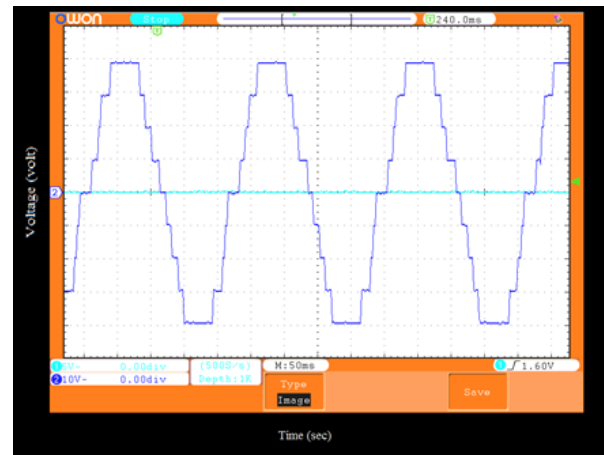


Fig.37. DSO Output Waveform of Nine Level Inverter

Fig.38. shows the experimental arrangement with DSO for the modified nine level MLI and thus obtained the nine level output voltage across the load resistor. In the experimental setup it consists of power circuit, driver circuit and controller board.

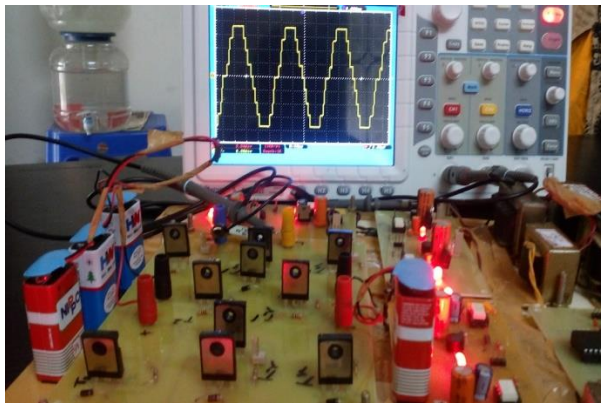


Fig.38. Experimental Setup with Nine Level

The developed prototype of the proposed multilevel inverter produces a voltage level of nine with $\pm 36\text{V}$ as the output voltage for a given input of 9V and 27V. With this developed prototype it possess lesser components count and it have lower THDs.

CONCLUSION

Modified DSTATCOM based nine level multilevel inverter has been developed and the simulation model is verified using MATLAB/Simulink. As interest in MLI grows, efforts are being made to reduce the number of devices in order to increase the number of output levels, Known as a switched DC source topology as part of this topology, it was developed to reduce the number of devices. Instead of using a cascading inverter topology, it is better because the switch DC source topology control is less complex, less costly, and has a lower THD percentage. This topology can only be effectively used by applications that can use an isolated DC source. Several MLI studies have been conducted in place of this, and these studies have been used to compare different topologies. Based on these studies, new DSTATCOM multi-level inverters that use addition and subtraction topologies can be developed. Implementing this topology eliminates the shortcomings

of switching DC source topologies and improves stability. In addition to these multi-carrier PWM modulation techniques, uniform switches can be leveraged and applied for uniform power distribution. With the proposed topology, a hardware prototype was developed and the hardware results were obtained. Finally, we will compare the existing multi-level inverter with the modified multi-level inverter.

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